IN THE CLAIMS:

Please cancel claims 2, 11 and 19, and amend claims 1, 3, 6 - 12 and 15 - 18 as follows:

1. (Currently Amended) A control loop circuit for optimizing a power supply output under varying load conditions, the power supply having a main loop amplifier and an output stage to generate the output, the control loop circuit including:

a first control path ~~having a predetermined level of linear compensation, the first control path~~ coupled to the output and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a second control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the second control path ~~having an output coupled to the main loop amplifier output.~~comprising

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the digital-signal-processor operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

2. (Cancelled)

3. (Currently Amended) A control loop circuit according to claim ~~2~~ 1 wherein:

the look-up table comprises a RAM memory.

4. (Previously Amended) A control loop circuit according to claim 1 wherein the second control path is disposed in parallel with the first control path.

5. (Previously Amended) A control loop circuit according to claim 1 wherein:

the second control path is selectively activated when the error signal is greater than a predetermined threshold.

6. (Currently Amended) A control loop circuit according to claim ~~2~~ 1 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

7. (Currently Amended) A control loop circuit according to claim ~~2~~ 1 wherein:

the first control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

8. (Currently Amended) A control loop circuit for controlling the loaded output of a DUT power supply, the DUT power supply including an input, a main loop amplifier and an output stage amplifier, the control system including:

means for ~~statically~~ compensating an error signal, the means for ~~statically~~ compensating coupled between the input and output of the power supply; and

a dynamic compensation control loop including a digital-signal-processor, the dynamic compensation control loop disposed in parallel with the means for ~~statically~~ compensating, the dynamic compensation control loop selectively cooperating with the means for ~~statically~~ compensating to optimize the power supply output in response to varying output loads.

9. (Currently Amended) A control loop circuit according to claim 8 wherein:

the means for ~~statically~~ compensating an error signal comprises a first control path ~~having a predetermined level of linear compensation, the first control~~

~~path~~ including an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier.

10. (Currently Amended) A power supply system including:

a main loop amplifier circuit;

an output stage disposed in cascade with the main loop amplifier circuit; and

a control loop circuit, the control loop circuit including

a first control path ~~having a predetermined level of linear compensation, the first control path~~ coupled to the output stage and having an error amplifier, the error amplifier operative to generate an error signal for presentation to the main loop amplifier, the error signal representing the difference between a desired output and a sensed output; and

a second control path coupled to the error amplifier output and responsive to the error signal to generate a dynamic compensation signal, the second control path ~~having an output coupled to the main loop amplifier output.~~comprising:

input conversion circuitry for converting the error signal into a digital signal,

a digital-signal-processor coupled to the conversion circuitry;

a look-up table for storing optimal compensation signal responses to detected error signals, the digital-signal-processor operative in response to the digitized error signal to access the look-up table and identify the optimal compensation signal, and generating the optimal signal; and

output conversion circuitry for feeding the optimal signal to the main loop amplifier output.

11. (Cancelled)

12. (Currently Amended) A power supply system according to claim ~~11~~ 10 wherein:

the look-up table comprises a RAM memory.

13. (Previously Amended) A power supply system according to claim 10 wherein the second control path is disposed in parallel with the first control path.

14. (Previously Amended) A power supply system according to claim 10 wherein:

the second control path is selectively activated when the error signal is greater than a predetermined threshold.

15. (Currently Amended) A power supply system according to claim ~~11~~ 10 wherein:

the output conversion circuitry comprises a digital-to-analog converter.

16. (Currently Amended) A power supply system according to claim ~~11~~ 10 wherein:

the first control path includes respective source and sink signal paths; and

the output conversion circuitry comprises respective source and sink digital-to-analog converters coupled to the respective source and sink signal paths.

17. (Currently Amended) A method of controlling the output of a DUT power supply, the method including the steps of:

generating a ~~statically~~ first compensated error signal based on the difference between the desired power supply output and the actual power supply output;

producing a dynamically compensated error signal in parallel with the ~~statically~~ first compensated error signal, the producing step further comprising~~; and~~

converting the first compensated error signal into a digital signal;

analyzing the digital signal;

creating a digital dynamically compensated error signal based on the analyzing step;

converting the digital dynamically compensated error signal to an analog dynamically compensated error signal; and

summing the ~~statically~~ first compensated error signal and the dynamically compensated error signals to create an optimal compensation signal.

18. (Currently Amended) A method according to claim 17 wherein the producing step is dependent on the magnitude of the ~~statically~~ first compensated error signal being above a pre-set threshold.

19. (Cancelled)